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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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*Ex parte* SIMON CHARLES WATT and LUC ORION

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Appeal 2008-5801
Application 10/714,483
Technology Center 2100

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Decided:[1] March 31, 2009

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Before HOWARD B. BLANKENSHIP, JAY P. LUCAS, and THU A. DANG, *Administrative Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

## STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-39, which are all the pending claims. We have jurisdiction under 35 U.S.C. § 6(b). Oral argument by Appellants' representative was heard on March 18, 2009.

We affirm.

### *Invention*

Appellants' invention relates to a method of controlling a monitoring function of a processor that is operable in at least two (e.g., secure and less secure) domains. (*See* Abstract.)

### *Representative Claim*

1. A method of controlling a monitoring function of a processor, said processor being operable in at least two domains, comprising a first domain and a second domain, said first and second domains each comprising at least one mode, said method comprising the steps of:

controllably monitoring said processor operating in each of said at least two domains,

setting at least one control value, said at least one control value relating to a condition and being indicative of whether said monitoring function is allowable in said first domain;

allowing initiation of said monitoring function in said first domain when said condition is present if its related control value indicates that said monitoring function is allowable; and

not allowing initiation of said monitoring function in said first domain when said condition is present and its related control value indicates that said monitoring function is not allowable.

*Prior Art*

The Examiner relies on the following references as evidence of unpatentability.

| | | |
|---|---|---|
| Christensen | US 5,752,013 | May 12, 1998 |
| Angelo | US 6,581,162 B1 | Jun. 17, 2003 |
| Faccin | US 6,879,690 B2 | Apr. 12, 2005 |
| Alverson | US 7,020,767 B2 | Mar. 28, 2006 |

*Examiner's Rejections*

Claims 1-8, 11-16, 18-36, 38, and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Alverson and Angelo.[2]

Claims 9, 10, 17, and 37 stand rejected under 35 U.S.C. § 103(a) over Alverson, Angelo, and "common art."

[2] The Answer (at 3) erroneously lists claim 10, which depends from claim 9, as being unpatentable over the first-stated combination.

*Claim Groupings*

Based on Appellants' arguments in the Appeal Brief, we will decide the appeal on the basis of claims 1, 9, and 20. See 37 C.F.R. § 41.37(c)(1)(vii).

## FINDINGS OF FACT

*Angelo*

1. Angelo describes a secure environment for entering and storing information necessary for encryption processes, using the secure memory space provided by System Management Mode (SMM) memory. Angelo Abstract.

2. According to Angelo, SMM is entered upon receipt of a system management interrupt (SMI). Conventionally, SMIs were used for power management in portable systems. Angelo col. 7, ll. 40-55.

3. SMIs are asserted by an SMI timer, by a system request, or by other means. *Id.*, ll. 56-57.

4. An SMI is a non-maskable interrupt of very high priority. Only the reset signal and the cache flush signal have higher priority. *Id.*, ll. 57-61.

5. When an SMI is asserted, a microprocessor maps SMM memory into the main memory space. The entire CPU state is saved in SMM memory, after which an SMI handler routine services the interrupt. *Id.*, col. 7, l. 61 - col. 8, l. 4.

6. While the SMI handler routine is executing, other interrupt requests are not serviced, but ignored. *Id.*, col. 8, ll. 4-7.

7. The SMI handler can be written to perform tasks other than the original power management tasks. Because SMM memory is only addressable while the computer system is in SM mode, critical information entered into the memory is secure. *Id.*, col. 8, ll. 39-52.

8. Angelo discusses a procedure (Fig. 5) for securely obtaining a single character from the keyboard to placement in secure memory. A request for secure keyboard communications causes the computer's processor to enter into SMM, so that the SMI handler can ensure that entered data is stored in secure memory. *Id.*, ll. 53-66.

9. The procedure of Figure 5 may begin when the computer system detects a request for secure communications. *Id.*, col. 9, ll. 3-6.

10. Control proceeds to step 402 (Fig. 5), where appropriate registers in the processor are loaded prior to execution of the SMI code. *Id.*, ll. 6-8.

11. The register values indicate a request for secured keyboard communications. *Id.*, ll. 8-9.

12. Control proceeds to step 404 (Fig. 5), where an application generates a "soft" SMI (a software interrupt), which places the processor in SMM. *Id.*, ll. 9-13.

13. The processor executes the SMI handler routine. *Id.*, ll. 22-24.

14. The SMI handler examines the processor registers to determine what type of process (e.g., secure keyboard request) initiated the request, and performs accordingly. *Id.*, ll. 24-29.

15. One skilled in the art would have understood that, when the processor register values indicate that an SMI should be generated (FF 11, 12), SMM may be entered (FF 12), but would not be entered when an interrupt of higher priority (e.g., FF 4) is present.

16. One skilled in the art would have known that the processor also handles other system requests, in addition to the SM interrupt.

## PRINCIPLES OF LAW

A person having ordinary skill in the art uses known elements for their intended purpose. *Anderson's-Black Rock, Inc. v. Pavement Salvage Co.,* 396 U.S. 57 (1969) (radiant-heat burner used for its intended purpose in combination with a spreader and a tamper and screed).

"[W]hen a patent 'simply arranges old elements with each performing the same function it had been known to perform' and yields no more than one would expect from such an arrangement, the combination is obvious." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740 (2007) (quoting *Sakraida v. Ag Pro, Inc.*, 425 U.S. 273, 282 (1976)).

ANALYSIS

The Examiner finds that the SMI taught by Angelo corresponds to the "control value" recited in instant claim 1. Appellants acknowledge (App. Br. 10) that entry into the SMM as taught by Angelo is a "monitoring function." (*See also* Ans. 15.) However, Appellants allege that the function is always allowed in response to an SMI. (App. Br. 10.)

Although Appellants' allegation is irrelevant to the rejection, the allegation is unfounded. Angelo teaches that the function is usually, *but not always*, allowed in response to an SMI. (*See* FF 15).

The Examiner further finds that the control value (SMI interrupt) is related to several "conditions" that meet the terms of instant claim 1. (Ans. 14; *see* FF 3.) Appellants allege that the term "condition" has some (unidentified) special meaning in the art (Reply Br. 2), but do not refer us to any evidence in support of the allegation, nor tell us what that the unsupported, unidentified special meaning may be. Appellants also refer to a "number of embodiments" in the Specification and seem to assert that some (unidentified) special meaning of "condition" can be gleaned from the described embodiments (*see id.*), which, presumably, would distinguish over the conditions in Angelo that were identified by the Examiner. Thus, although Appellants allege (*id.*) there is a "definition" for the term "condition" set out in the Specification, Appellants not only do not tell us where the definition may be found, but also neglect to tell us what that the definition may be.

We will not, and cannot, read any of the specific embodiments described in the Specification into instant claim 1. The *claims* measure the invention. *See SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). Our reviewing court has repeatedly warned against confining the claims to specific embodiments described in the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc). During prosecution before the USPTO, claims are to be given their broadest reasonable interpretation, and the scope of a claim cannot be narrowed by reading disclosed limitations into the claim. *See In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997); *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989); *In re Prater*, 415 F.2d 1393, 1404-05 (CCPA 1969). "An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process." *In re Zletz*, 893 F.2d at 322.

In any event, the Examiner finds that one of the "conditions" taught by Angelo is a system request. (Ans. 14.) Angelo describes a secure user mode (FF 8-14). Register values in the processor are loaded to indicate the condition of the secure user mode (FF 10-11). A system request, in response to the request for secure user mode, subsequently generates an interrupt (asserts the SMI) and enters the system into SM mode (FF 12).

However, other interrupt requests, in addition to the SMI, are serviced by the processor (FF 6, 16). Angelo thus teaches allowing initiation of the

monitoring function in the first domain when the condition (system request) is present if its related control value indicates that the monitoring function is allowable (system request to assert SMI; SMI is asserted), and not allowing initiation of the monitoring function in the first domain when the condition (system request) is present and its related control value indicates that the monitoring function is not allowable (system request to assert some other interrupt; SMI not asserted).

Appellants' claim 1 sets no limitation on the substance of the "control value," but provides some kind of abstract, sideways definition by reference to what the value may be "relating to" or "indicative of." In claim 1, the "control value" is "indicative of" only two states -- allowable or not allowable. The claimed "control value" can be a signal level, as Appellants seem to acknowledge at pages 3 and 4 of the Reply Brief. However, the "control value" can also be an element in a processor register that causes the signal level to be asserted (FF 10-11), or an element in program memory that causes the application to generate the particular (SMI) software interrupt (*see* FF 12).

With respect to claim 20, Appellants argue that Angelo does not teach a "storage element" operable to be set to contain at least one control value. (App. Br. 6-7.) We disagree. (*See* FF 10-12.) Angelo teaches a "storage element" --registers in the processor -- operable to be set to contain at least one control value -- one or more bits that indicate an SM interrupt is to be asserted.

Appellants also allege (App. Br. 9) that the Examiner has not shown where the "not allowing" step of claim 1 or the "control logic" of claim 20 is taught by the references. In Appellants' only response to more specific findings set out by the Examiner (Ans. 16-17), Appellants repeat the allegation that Angelo teaches the "direct opposite," or is "diametrically opposite," to what is specified in Appellants' claims. (Reply Br. 6.) Appellants' remarks are not persuasive of error in the rejection of claim 1 or claim 20, because Appellants have not shown that Angelo teaches anything "opposite" to what is claimed.

With respect to the rejection of claim 9 over Alverson, Angelo, and "common art," the "common art" takes the form of official notice that "saving instruction traces is [sic; was] common in the art and can be utilized for many debugging purposes." (Final Rej. 11; Ans. 12.)

Appellants contend they have "traversed" the Examiner's taking of official notice. (App. Br. 11, 13.) However, the "traversal" consists of pointing out that the Examiner failed to cite any supporting evidence. (*See* App. Br. 11.) Appellants' "traversal" thus takes the form of pointing out that the official notice is official notice.

The USPTO may take notice of facts beyond the record which, while not generally notorious, are capable of instant and unquestionable demonstration as to defy dispute. *In re Ahlert*, 424 F.2d 1088, 1091 (CCPA 1970). In the instant case, Appellants have not traversed the Examiner's official notice. A "traverse" is not pointing out that the Examiner has not

provided supporting evidence for the official notice. Nor is a "traverse" a demand for evidence. A "traverse" is a denial of an opposing party's allegations of fact. *See Black's Law Dictionary Fifth Edition* ("In common law pleading, a traverse signifies a denial."). Moreover, an *adequate* traverse must contain adequate information or argument to create on its face a reasonable doubt regarding the circumstances justifying the official notice. *In re Boon*, 439 F.2d 724, 728 (CCPA 1971).

In response to Appellants' concerns, although under no obligation to do so, the Examiner cited two prior art patents in support of the official notice. (Ans. 18.) Appellants do not deny that saving instruction traces was common in the art and could be utilized for many debugging purposes (*see* App. Br. 11; Reply Br. 7-8). Nor do Appellants assert that the Examiner's cited evidence fails to support the official notice (*see* Reply Br. 7-8). Appellants merely submit that the Examiner "must provide some 'rationale' or 'motivation' for combining those new references with the Alverson/Angelo combination." (Reply Br. 8.)

We disagree that the Examiner must provide some "rationale" or "motivation" for combining the newly cited references with Alverson and Angelo. The Examiner finds that the artisan would have been motivated to use the known technique of saving instruction traces to gather more debugging or security information for analysis. (App. Br. 12.) The Examiner further finds that it would have been obvious to one of ordinary skill in the art to include a trace enable bit to indicate to the processor that

instruction traces are to be saved. (*Id.*) Appellants have done nothing to call these findings into question, nor alleged that the proposed combination would not result in the claimed invention other than, perhaps, the alleged lack of "relating to" and "indicative of" that we have previously considered.

Finally, Appellants allege that "at no point in the rejection" does the Examiner provide the required "reason" or "motivation" for combining the Alverson and Angelo references. (App. Br. 12.) However, the Examiner finds that, with the knowledge evidenced by Alverson and Angelo, the ordinary artisan would have been motivated to use the techniques taught by Angelo in computer security memory management, with domain-specific multiple levels of protection. (Ans. 3.)

Appellants submit in response that "Alverson has no suggestion that combining it with portions of Angelo or other references would provide any benefit at all if or when portions where [sic] combined with portions of Alverson." (Reply Br. 9.) Appellants do not allege that anything about the proposed combination might be deficient, other than the lack of specific suggestion in one reference or the other for the combination (*see* Reply Br. 8-10).

Presumably, Appellants know there is no requirement that one reference provide a specific suggestion to combine some elements with some other elements in another reference. Appellants seem to submit the remarks in response to the Examiner's reference to what, for example, "Alverson" would have been motivated to do (*see* Ans. 3). However,

Appellants could not have been misled into the belief that the rejection is based on what would have been obvious to some unidentified entity (e.g., "Alverson"), because the rejection is under 35 U.S.C. § 103. The statute is specific with respect to what would have been obvious "to a person having ordinary skill in the art."

Thus, for the claims we have reviewed, Appellants have not shown that the invention does anything more than simply arrange old elements with each performing the same function it had been known to perform, yielding no more than one would expect from such an arrangement, and thus an obvious combination. *See KSR* at 1740.

We have considered all of Appellants' arguments in response to the rejections. We are not persuaded that any of the claims have been rejected in error. We sustain the § 103(a) rejections of claims 1-39.

## DECISION

The rejection of claims 1-8, 11-16, 18-36, 38, and 39 under 35 U.S.C. § 103(a) as being unpatentable over Alverson and Angelo is affirmed.

The rejection of claims 9, 10, 17, and 37 under 35 U.S.C. § 103(a) over Alverson, Angelo, and "common art" is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

rwk

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